ELECTRONIC INFORMATION DISCLOSURE STATEMENT

Electronic Version v18

Stylesheet Version v18.0

Title of Invention	SELF-ALIGNED DRAIN/CHANNEL JUNCTION IN VERTICAL PASS TRANSISTOR DRAM CELL DESIGN FOR DEVICE SCALING

Application Number :

Confirmation Number:

First Named Applicant: Geng Wang

Attorney Docket Number: FIS920030209US1

Art Unit:

Examiner:

Search string: (6414347 or 6440793 or 20020096219).pn

US Patent Documents

Note: Applicant is not required to submit a paper copy of cited US Patent Documents

init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass
	1	6414347	2002-07-02	Divakaruni			
	2	6440793	2002-08-27	Divakaruni			

US Published Applications

Note: Applicant is not required to submit a paper copy of cited US Published Applications

init	Cite.No.	Pub. No.	Date	Applicant	Kind	Class	Subclass
	1	20020096219	2002-03-11	Chidambarrao			

Signature

Examiner Name	Date